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(54) **An ultra dense DRAM cell array and its method of fabrication.**

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Description

This invention relates generally to dynamic random access semiconductor memory arrays and more specifically relates to an ultra dense dynamic random access memory array. It also relates to a method of fabricating such arrays using a plurality of etch and refill steps which includes a differential etching step which is a key step in forming insulating conduits which themselves are adapted to hold a pair of field effect transistor gates of the adjacent transfer devices of one device memory cells. The differential etch step provides spaced apart device regions and an insulation region of reduced height between the trenches which space apart the memory cells. After isolating each device region with insulation, the spacing trenches and the insulation region of reduced height are refilled with conductive material. A subsequent etch step which brings the polycrystalline silicon below the level of the insulation region of reduced height sets the stage for the formation of gate conduits between columns of memory cells. An oxide formation step then forms an oxide on the etched polycrystalline silicon bringing it to the same level as the height of the insulation region of reduced height forming a continuous conduit of insulation material having substantially the same level across the array. After formation of a pair of gates in each of the thus formed conduits, the gates within each conduit are electrically isolated from each other, a device region in each of the memory cells is implanted to complete a field effect transistor transfer device and bitline metallization is formed to interconnect rows of memory cells. The lowermost portions of the device regions act as extended drains forming one electrode of a charge storage capacitor.

The resulting structure includes a plurality of rows of vertically arranged field effect transistors wherein the substrate effectively acts as a counterelectrode surrounding the insulated drain regions of each of the one device memory cells. A pair of gates are disposed in insulating conduits which run perpendicular to the rows of memory cells. Each gate in a conduit is disposed in insulated spaced relationship with a memory cell channel region which, in response to signals on the gate turns on a column of channel regions so as to permit the entry of charge into a selected storage region when a bitline associated with a particular cell is energized. The resulting array shows rows of pairs of memory cells wherein each cell of a pair is spaced from the other by a portion of the substrate acting as a counterelectrode and each of the pairs of memory cells is similarly separated from an adjacent pair by regions of conductive material acting as a counterelectrode. Of course, each row of memory cells is separated from adjacent rows by rows of dielectric material which include regions of reduced height which also form part of the conduits in which cell wordlines are disposed.

The formation of trenches using various masking and etching techniques is well-known in the prior art. Similarly, the refilling of trenches for isolation and device forming purposes is also well-known. An article entitled "Self-Aligning Multi-Depth Trenches" in the IBM Technical Disclosure Bulletin, Vol. 28, No. 3, August 1985, page 1235 shows the formation of orthogonally disposed deep and shallow trenches which can be refilled with a suitable material. In the article, the trenches are used to obtain both deep and shallow isolation. The isolated epitaxial areas are subsequently utilized to form bipolar devices.

U.S. Patent 4,520,553, filed January 16, 1984, shows a semiconductor device with a deep grid accessible via the surface having a silicon substrate and comprising U-shaped grooves. The upper parts of the sidewalls of the grooves are insulated by a silicon layer and the lower parts of the grooves connect up with heavily doped zones. Polycrystalline silicon provides ohmic contact between selected positions on the upper face of the transistor and the grid layer. The reference basically shows the formation of grooves, filling with polysilicon and outdiffusing to provide dopant regions at the bottom of the grooves. While there are interconnections between rows of devices, there are no connections between devices in an orthogonal direction. Differential etching is not contemplated in the method of this reference.

U.S. Patent 4,510,016, filed December 9, 1982, shows a submicron structure including a plurality of fingers which are thinned down by the repeated oxidation and stripping of the walls of a U-shaped groove. In this reference a portion of each of the devices is formed by etching grooves in a semiconductor. The regions between the grooves are left open so that in a subsequent metallization step both emitter and self-aligned Schottky barrier contacts can be formed. The spacing between the devices is in only one direction.

An abstract of Japanese Patent 59-19366, filed January 31, 1984, shows a vertical field effect transistor memory cell disposed within an isolation region which is itself formed in a semiconductor substrate counterelectrode. In this arrangement, a groove is formed in the semiconductor substrate which is refilled with polycrystalline silicon. After planarizing, layers of semiconductor from which a channel region and source of an FET device are to be formed are disposed atop the polished polycrystalline. To the extent that the layers formed on the polycrystalline semiconductor are themselves polycrystalline in character, these layers must be rendered single crystal by a technique called laser recrystallization. Further masking and etching steps form a pedestal of these layers which are then surrounded with insulating material up to the level of the polycrystalline in the mesa. A polycrystalline silicon gate is then disposed in insulated spaced relationship with the channel region. The gate is then electrically insulated and metallization applied to the single crystal semiconductor

source region to form bitlines which are disposed orthogonal to the polycrystalline gate which forms a wordline for a column of similar memory cells. Thus, while a vertical device is formed, its structure and method of fabrication are such that techniques like laser recrystallization must be invoked providing, at best, epitaxial regions of questionable quality for the transfer device of each memory cell. In the technique just described, a straightforward etch and refill technique is involved without invoking the differential etch technique of the present application.

US-A-4 737 829 discloses a DRAM cell array where said cells are formed in an array of protrusions formed in a Si substrate. Said cells are not dielectrically isolated from the Si substrate. EP-A-0 198 590 also discloses a DRAM cell array with cells formed in silicon islands, being said cells not dielectrically isolated from the substrate.

It is, therefore, an object of the present invention to provide according to claim 9 an ultra dense DRAM memory array wherein each memory cell is made of a vertical single crystal, device regions wherein the single crystal material requires no special technique to form it other than epitaxial disposition and etching.

Another object is to provide a method according to claim 1 for forming an ultra dense DRAM memory array wherein a differential etching step is utilized to simultaneously etch two different materials at different rates such that transistor device regions are formed and the height of insulating conduits to be formed subsequently is predetermined.

Still another object is to provide an ultra dense DRAM memory array wherein the width of the active device region is defined by a spacer smaller than the lithographic limit.

Yet another object is to provide an ultra dense memory array wherein pairs of wordlines are formed in insulating conduits portions of which are formed from isolation regions of reduced height and other portions of which are formed from oxidized portions of a common conductive counterelectrode.

This invention relates to an integrated circuit memory array which contains a plurality of vertically arranged memory cells and to its method of fabrication. The memory array includes a plurality of dynamic random access memory (DRAM) cells which are vertically arranged field effect transistors. Each portion of the field effect transistors is formed from epitaxially deposited, single crystal semiconductor material. Each transistor has an extended drain region which is disposed in insulated spaced relationship with a common counterelectrode which is connected to the substrate. Wordlines are spaced from the channel region of associated transistors by means of gate oxides and pairs of such wordlines are disposed in gate conduits in insulated spaced relationship with the material that forms the counterelectrode. The wordlines are buried in oxide which partially supports orthogonally disposed bitlines which contact the exposed implanted sources of each of the field effect transistors.

The above described structure is formed by first etching trenches in underlying substrate regions which are spaced from each other by an oxide layer. The trenches are filled with insulating material. The resulting structure is then masked and differentially etched so that a plurality of rows of trenches are formed in the substrate portions and oxide spacer regions. Simultaneously, the unmasked portions of the previously formed insulation is reduced in height to a desired level during the etching of the rows of trenches. In a succeeding step, the trench walls are covered with insulation and the trenches and the regions over the reduced height insulation regions are refilled with semiconductor material. The refilled semiconductor is then etched down to a desired height in certain of the refilled trenches, covered with an oxide and the resulting trench is conformally covered with conductive material. In a subsequent step, the conductive material is etched leaving pairs of gate conductors extending orthogonally to the rows of field effect transistors. After burying the gate conductors which act as wordlines for adjacent field effect transistors, source regions are formed and bitline metallization is formed on the exposed sources completing the fabrication of an ultra dense DRAM memory array.

The foregoing and other objects, features and advantages of the present invention will become more apparent from the following more particular description of a preferred embodiment, depicted in the drawings in which:

Fig. 1 is a cross-sectional perspective view of an integrated circuit memory array which contains a plurality of vertically arranged memory cells.

Fig. 2 is a top view of the memory array of Fig. 1 showing the layout of the Dynamic Random Access Memory (DRAM) cells and their associated polycrystalline silicon gates and bitlines. Oxide isolation is shown extending between rows of memory cells.

Fig. 3 shows a cross-sectional view of the memory array of Fig. 1 at an intermediate stage in its fabrication.

Fig. 4 is a cross-sectional view of the structure of Fig. 3 after it has been subjected to photolithographic, etching and oxidation steps.

Fig. 5 shows the structure of Fig. 4 after it has been subjected to a further reactive ion etching step.

Fig. 6 shows the structure of Fig. 5 in perspective after it has been subjected to a trench refill, planar-

izing and polishing steps.

Fig. 7 shows a cross-sectional perspective view of a portion of the memory array of Fig. 1 after its polished surface has been subjected to further processing steps.

Fig. 8 is a cross-sectional perspective view of Fig. 7 on a slightly expanded scale after the structure of Fig. 7 has been subjected to reactive ion etching.

Fig. 9 is a cross-sectional view of that portion of Fig. 8 taken along line 9-9 of Fig. 8.

Fig. 10 is a cross-sectional view of Fig. 8 at a later intermediate stage in its fabrication.

Fig. 11 shows the structure of Fig. 10 at a still later intermediate stage in its fabrication after the semiconductor trenches and reduced height insulation regions have been refilled with polycrystalline silicon.

Fig. 12 is a cross-sectional view taken along line 12-12 of Fig. 11 showing isolation oxide regions of reduced height surrounded by polycrystalline silicon.

Fig. 13 shows a cross-sectional view of Fig. 11 at a still later intermediate stage in its fabrication.

Fig. 14 shows a cross-sectional view of Fig. 13 after polycrystalline silicon device gates have been formed.

Fig. 15 shows a cross-sectional view of Fig. 14 after the surface of the memory array has been planarized, source regions have been ion implanted and the bitline metallization deposited and patterned.

Fig. 1 is a cross-sectional perspective view of an integrated circuit memory array which contains a plurality of vertically arranged memory cells in accordance with the teaching of the present invention. Memory array 1 includes a plurality of dynamic random access memory (DRAM) cells 2 which are vertically arranged field effect transistors. Each cell 2 includes an n conductivity type source region 3, a p conductivity type channel region 4 and an extended n conductivity type drain region 5. A polycrystalline silicon gate 6 is shown in Fig. 1 disposed in insulated spaced relationship with an associated channel region 4 by means of a gate oxide 7 for each cell 2. Extended drain region 5 is also disposed in insulated spaced relationship with n^+ conductivity type silicon substrate 8 by means of an oxide layer 9. Gates 6 are shown in Fig. 1 disposed on insulating oxide regions 10 which space them from n^+ polycrystalline silicon regions 11. The latter regions are in direct contact with an n+ single crystal silicon semiconductor substrate 8 which ties all the n^+ polycrystalline regions 11 together. Another n^+ polycrystalline region 12 is shown in Fig. 1 disposed between cells 2 and spaced from them by composite nitride/oxide insulating elements 13. Similar elements 13 space cells 2 from insulating oxide regions 10 and n^+ polycrystalline silicon regions 11. Polycrystalline silicon region 12 is capped with an oxide layer 14 and the regions between and over polycrystalline silicon gates 6 are filled with a flat topped, CVD oxide region 15. Conductive bitlines 16 are disposed orthogonally to gates 6 and extend from one side of memory array 1 to the other. In Fig. 1, bitlines 16 are connected to source regions 3 of DRAM cells 2. Thus, bitlines 16 are connected to rows of memory cells 2 and apply one of the potentials required to store information in the extended drain regions 5 of cells 2 which also act as one electrode of a storage capacitor. In the arrangement of Fig. 1, n^+ polycrystalline regions 11,12 act as the other electrode of the storage capacitor. In Fig. 1, rows of memory cells 2 are spaced from each other by oxide isolation regions 17 which extend across memory array 1 in a direction parallel to bitlines 16 and perpendicular to gates 6. Flat topped CVD oxide regions 15 extend over the flat tops of isolation regions 17' and along with oxide layer 14, support bitlines 16 in insulated spaced relationship from each other except where they contact source regions 3. As with all memory cells of the character just described, wordlines 6, when selected, have an appropriate potential applied thereto which switches the selected memory cell 2 to store a digital "1" or "0". A selected bitline 16, as suggested hereinabove, applies a desired potential to all of source regions 3 of memory cells 2 in the selected row and that potential along with the selected gate 6 selects one memory cell 2 out of all the available memory cells in a well-known manner.

Referring now to Fig. 2, there is shown therein a top view of memory array 1 showing the layout of DRAM cells 2 and their associated polycrystalline silicon gates 6 and bitlines 16. Oxide isolation regions 17 and 17' are also shown extending from one side of array 1 to the other.

Integrated circuit array of memory cells shown in FIGS. 1 and 2 may be fabricated into a highly dense array which, because of the vertical positioning of memory cells 2, is not subject to deleterious short channel effects.

Fig. 3 shows a cross-sectional view of memory array 1 at an intermediate stage in its fabrication process. In an initial series of steps, n^+ conductivity type silicon substrate 8 is covered with an oxide layer 20 portions of which remain in the final structure as oxide layer 9. Another n^+ substrate 21 which contains a p^- region 22 is bonded with oxide layer 20 in a manner well-known to those skilled in the semiconductor fabrication art. One way of achieving such bonding is shown in an article entitled "Silicon-On-Insulator (SOI) By Bonding and Etch-Back" by J. Lasky et al, IEDM 85, page 684. A layer of silicon nitride 23 and a layer of chemically vapor deposited silicon dioxide 24 are deposited on the surface of layer 22 which may have been previously epitaxially deposited or ion implanted or diffused to render it of p^- conductivity type.

Fig. 4 is a cross-sectional view of the structure of Fig. 3 after it has been subjected to photolithographic, etching and oxidation steps which form oxide covered trenches which extend through p^- region 22 into n^+ substrate 21. In Fig. 4, trenches 25 are formed by first depositing a photoresist, patterning and developing it. The exposed portions of oxide layer 24 and nitride layer 23 are removed by a Reactive Ion Etching (RIE) step using CF_4+H_2 as an etchant gas. After the remaining photoresist is removed, memory array 1 is subjected to an RIE step which etches through the unmasked portions of p^- layer 22 and into n^+ substrate 21. The resulting trenches 25 are then subjected to a thermal oxidation step which forms a thermal oxide layer 26 on the walls of trenches 25. Semiconductor substrate 21 and p^- region 22 are reactively ion etched using Cl_2+O_2 as an etchant gas in a well-known way.

Fig. 5 shows the structure of Fig. 4 after it has been subjected to a further reactive ion etching step. In Fig. 5, that portion of thermal oxide layer 26 which is disposed on the bottom of trench 25 is first removed by subjecting it to a reactive ion etching step using CF_4+H_2 to etch the oxide in a well-known manner. After the oxide on the bottom of trench 25 is removed, reactive ion etching is continued using Cl_2+O_2 to etch the semiconductor of n^+ substrate 21 down to oxide layer 20. At this point, the etchant gas is changed to CF_4+H_2 to reactively ion etch oxide layer 20. Once layer 20 has been penetrated, the etchant gas is changed to Cl_2+O_2 to penetrate into substrate 8 to a depth which will be approximately the same depth as the depth of trench capacitors which will be formed in subsequent steps.

Referring now to Fig. 6, the structure of Fig. 5 is shown in perspective after it has been subjected to a trench refill and planarizing and polishing steps. After trenches 25 have been reactively ion etched to the desired depth, a thermal oxide (not shown) is grown on the unoxidized portions of the trench sidewalls. After this, trenches 25 are refilled with a chemically vapor deposited oxide using TEOS or other well-known chemical vapor deposition technique. Then, using the remaining portions of nitride layer 23 as an etch stop, the chemically vapor deposited oxide in trenches 25 is chemically-mechanically polished to provide the planarized structure of Fig. 6. In Fig. 6, the chemically vapor deposited oxide is intended to be an oxide isolation which will extend across memory array 1 in a direction parallel to bitlines 16 and a portion of it, after further processing steps, will become oxide isolation regions 17 as shown in Fig. 2. To the extent that the character of the oxide isolation regions 17 in Fig. 6 do not change but will only be reduced in height due to the further processing steps, the reduced height portions will be designated by the reference character 17' where appropriate.

At this point in the fabrication process, memory array 1 has been converted through a plurality of masking and etching steps into a structure containing a plurality of oxide filled isolation trenches 17 which extend through an oxide layer 20 into an underlying silicon substrate 8. The height of array 1 is substantially unchanged at this point but, for purposes of orientation, it should be appreciated that oxide isolation regions 17 extend across array 1 in a direction parallel to bitlines 16 as shown in Fig. 1.

Referring now to Fig. 7, there is shown a cross-sectional, perspective view of a portion of memory array 1 after the polished surface of array 1 has been subjected to further processing steps. The perspective view shown in Fig. 7 is orthogonal to the view shown in Fig. 6. After the polishing step described in connection with Fig. 6, layers of silicon nitride 27, CVD oxide 28 and silicon nitride 29 are deposited in a well-known way in succession. Nitride layer 29 is shown in Fig. 7 after it has been patterned using well-known photolithographic and etching techniques. Nitride layer 29 is patterned so that the width and pitch size of the resulting nitride regions are larger than the minimum feature; larger than 0.5 microns, for example. After nitride layer 29 has been patterned, preferably by an RIE step using CH_3F+CO_2 as an etchant, a layer 30 of chemically vapor deposited polysilicon is formed having the configuration shown by the dashed lines in Fig. 7 which represent its shape prior to a reactive ion etching step. After being subjected to a reactive ion etching step, a plurality of polysilicon sidewall spacers 31 are formed alongside the portions of nitride layer 29 which remained after it was patterned. Spacers 31 are to be used to pattern oxide layer 28 and nitride layer 27 after the remaining portions of nitride layer 29 are removed using a suitable etchant such as phosphoric acid. Layers 27 and 28 are patterned using well-known etching techniques. The preferred way is using RIE with CF_4+H_2. At this point, portions of the silicon surface and the tops of insulation filled trenches 17 of memory array 1 are exposed. These exposed silicon and insulation regions are then subjected to a reactive ion etching step using Cl_2+O_2 as an etchant gas providing trenches 32 and insulation regions of reduced height 17', as shown in Fig. 8.

Other gas mixtures which may be used to achieve a differential etch rate between silicon and silicon dioxide are shown in TABLE I below. Using the different gas mixtures in a reactive ion etching mode, permits, as can be seen from TABLE I, the achievement of different etch rates for the two materials resulting in a process step which permits very accurate control of the final depth of trenches 32 and height of insulation region 17'.

RELATIVE REACTIVE ION ETCHING RATES OF:		GAS MIXTURE USED
Si	SiO_2	
1,2	1	CF_4
2~5	1	CF_4+O_2, CHF_3+O_2
5~10	1	CHF_3
>10	1	$Cl_2+BCl_3+He+O_2$ or $SiCl_4+Cl_2+BCl_3+He+O_2$

Fig. 8 is a cross-sectional, perspective view of Fig. 7 on a slightly expanded scale after the structure of Fig. 7 has been subjected to reactive ion etching using portions of layers 27,28 as masks. The resulting trenches 32 extend from the surface of array 1 through p^- region 22, n^+ substrate 21 and oxide regions 9 into n^+ substrate 8. As a result of the reactive ion etching step, a plurality of upstanding single crystal semiconductor regions are disposed on oxide regions 9 which prior to etching of trenches 32 formed portions of layer 20. Substrate 21 and p^- region 22 are intended to form portions of DRAM cells 2 and are shown in Fig. 1 as p conductivity type channel regions 4 and extended n conductivity type drain regions 5. Regions 4, 5 are shown by these same underlined reference characters 4, 5 in Fig. 8 to show the relationship of these regions to the structure of Fig. 1. The underlined reference characters will be used to identify the same regions in the following description.

At this point, a reference should be made to Fig. 6 which shows array 1 after isolation oxide 17 has been formed in trenches 25. It should be recalled that after the steps which formed isolation oxide regions 17, the height of array 1 was substantially unchanged from its initial starting height. Fig. 8 shows an isolation oxide region 17 having portions 17' of reduced height from those shown in Fig. 6. This results from the fact that during the reactive ion etching step which forms trenches 32, portions of the tops of isolation oxide region 17 were left unprotected intentionally to permit a reduction in the height of those unprotected portions of isolation oxide regions 17 to a desired level. A consideration of FIGS. 9 and 10 clearly shows that the height of isolation oxide regions 17 remains the same where they were protected by layers 27,28 and is reduced in regions where the underlying portions of memory array 1 have not been protected by layers 27,28.

Referring now to Fig. 9, there is shown a cross-sectional view of that portion of Fig. 8 taken along line 9-9 of Fig. 8. From Fig. 9, it should be clear that those regions of memory array 1 and isolation oxide regions 17 which are covered by layers 27, 28 are protected during the reactive ion etching step which forms trenches 32. In this manner, the upstanding regions 4, 5 are spaced from each other by isolation oxide regions 17 in a direction perpendicular to the direction of bitline 16 as shown in FIGS. 1 and 2. From the foregoing, it should be clear that by appropriate masking and using a single reactive ion etching step that both the height of isolation oxide regions 17 can be adjusted where desired to the height of oxide regions 17', for example, and the depth of trenches 32 controlled simultaneously.

Fig. 10 is a cross-sectional view of Fig. 8 at a later intermediate stage in its fabrication. Fig. 10 shows a composite oxide-nitride layer 13 formed on the sidewalls of trenches 32. A thin, n^+ polycrystalline silicon layer 33 is deposited on top of layer 13 to protect composite dielectric layers 13 during a subsequent reactive ion etching step.

Fig. 11 shows the structure of Fig. 10 at a still later intermediate stage in its fabrication. In Fig. 11, array 1 is subjected to another reactive ion etching step to remove polycrystalline layer 33 from the bottoms and sidewalls of trenches 32 and to remove those portions of composite layers 13 which are disposed on the bottoms of trenches 32. After the bottoms of trenches 32 are exposed, n^+ polysilicon 11,12 is deposited to fill in trenches 32. Fig. 11 shows the resulting structure after a chemical-mechanical polishing step is utilized to planarize the surface of array 1. In this latter step, nitride layers 27 act as etch stops. While not absolutely clear from Fig. 11, it should be appreciated that when polycrystalline silicon 11,12 is chemically deposited into trenches 32, polycrystalline silicon is also deposited on top of isolation oxide regions 17' which have been reduced in height due to a previous RIE step of isolation oxide regions 17.

Fig. 12 which is a cross-sectional view taken along line 12-12 of Fig. 11 shows isolation oxide regions 17' surrounded by polycrystalline silicon 11. The height reduction of isolation oxide regions 17 to isolation regions 17' of lesser height as has been previously indicated is a key part of the fabrication process because it ultimately allows for the formation of polysilicon gates all of which are connected together on a single level to form the memory array word lines.

Referring now to Fig. 13, there is shown a cross-sectional view of Fig. 11 at a still later intermediate stage in the fabrication of memory array 1. Fig. 13 shows a pair of insulating oxide regions 10 disposed atop n^+ polycrystalline regions 11. An oxide layer 14 is shown disposed atop n^+ polycrystalline region 12 which was formed at the same time as polycrystalline regions 11. Finally, Fig. 13 shows a layer 34 of n^+ polycrystalline silicon portions of which will remain after further fabrication steps as polycrystalline silicon gates 6 as shown in Fig. 1.

The structure of Fig. 13 is obtained by first carrying out a lithography step to provide a resist mask (not shown) to prevent etching of polycrystalline region 12. The unmasked n^+ poly regions 11 are then reactively ion etched until the level of the reduced height of oxide isolation regions 17' is reached. The reactive ion etching step leaves a polysilicon residue on composite nitride/oxide elements 13 which extend above region 11. After all the masking photoresist is removed, the polycrystalline silicon residue and about the same amount of poly over polycrystalline region 12 are removed by etching. The tops of polycrystalline regions 11 and 12 are then oxidized to provide insulating oxide regions 10 over the former and oxide layer 14 over the latter. During this oxidation step, only the polycrystalline silicon regions 11,12 will be oxidized since the nitride surface of composite oxide/nitride layers 13 prevents any further oxidation. At this point, the portions of composite elements 13 extending above oxide regions 10 are removed using well-known oxide and nitride etchants and a thin gate oxide 7 is thermally grown. Finally, a layer 34 of n^+ polycrystalline silicon is chemically vapor deposited in a well-known way over oxide region 10, oxide layer 14 and those portions of nitride layer 27 which remain over p conductivity type channel regions 4.

Fig. 14 shows a cross-sectional view of Fig. 13 after layer 34 of polycrystalline silicon has been reactively ion etched to form polysilicon spacers which are the polycrystalline gates 6 shown in Fig. 1. At this point, it should be noted that n^+ polycrystalline layer 34 has been deposited everywhere and, as such, forms over the surface of insulating oxide regions 10 and over the reduced height oxide isolation regions 17' which are approximately the same height as the polycrystalline silicon regions 11. Thus, when polycrystalline silicon layer 34 is subjected to a reactive ion etching step, the polycrystalline silicon sidewalls which remain extend across insulating oxide regions 10 and the surfaces of the reduced height oxide isolation regions 17' as shown in Fig. 1 forming the wordlines of memory array 1. The flat topped oxide regions 10 together with regions 17' form a plurality of gate conduits in each of which is disposed a pair of gates 6 which are completely insulated from any portion of substrate 8.

Referring now to Fig. 15, there is shown therein a cross-sectional view of Fig. 14 after the surface of array 1 has been planarized, source regions 3 have been ion implanted and the bitline metallization deposited and patterned.

After silicon gates 6 have been formed, silicon dioxide is chemically vapor deposited in a well-known way over the surface of array 1 burying polycrystalline gates 6 in oxide regions 15. The resulting surface is then planarized in a well-known way by chemical-mechanical polishing using nitride regions 27 as an etch stop. Nitride regions 27 are then removed using a selective etch, such as phosphoric acid, so that the surfaces of p conductivity type regions 4 are exposed. Arsenic is then ion implanted to form n conductivity type source regions 3. Finally, with source regions 3 exposed, metallization such as aluminum, a silicide forming metal or highly doped polycrystalline silicon is deposited on the surface of array 1. After patterning, bitlines 16 are formed interconnecting all of source regions 3 in a self-aligned manner. The resulting structure is shown in Fig. 1. The pattern of cells 2 repeats to the left and right of the cells shown in Fig. 1 such that after a polycrystalline region 11, another memory cell 2 is formed after which another polycrystalline region 12 is provided; the latter being followed by another memory cell 2.

The structure of Fig. 1 may be implemented to prove an ultra dense array of memory cells 2. The process used contemplates the fabrication of devices wherein wordlines 6 have a width of 0.1μm and the bitline width is in the range of 0.3~0.5μm. Isolation regions 17' and memory cells 2 have widths in the same range. The width of channel region 4 of each memory cell 2 is also in the 0.3~0.5μm range and because wordlines 6 overlap regions 4, the latter have slightly larger dimensions in the vertical direction.

To the extent that any semiconductor region of array 1 has been characterized as having a specific conductivity type, it should be appreciated that these same regions may be changed to opposite conductivity type. Thus, while devices 2 of memory array 1 have been characterized hereinabove as npn field effect transistors, devices 2 could equally well be pnp devices, operation of which is well-known to those skilled in the semiconductor fabrication arts.

Claims

1. A process for fabricating an ultra dense DRAM memory array containing a plurality of DRAM cells which process comprises the steps of:
forming a first plurality of trenches (25) in a semiconductor substrate (21) which is spaced from an underlying - at least semiconductive - substrate (8) by an insulating layer (20), said trenches (25) extending through said semiconductor substrate (21) and said insulating layer (20) into said underlying substrate (8),
refilling said plurality of trenches (25) with an insulating material (17),
forming a second plurality of trenches (32) orthogonally intersecting said first plurality of trenches (25), said trenches (32) extending through said semiconductor substrate (21) and said insulating layer (20) into said underlying substrate (8) to a predetermined depth, said first and second plurality of trenches (25, 32), respectively, defining a plurality of upstanding semiconductor regions for forming the active device regions of the said DRAM cells and, when forming said second plurality of trenches (32), portions of said insulating material (17) filling said first plurality of trenches (25) being excavated at the intersections of said second plurality of trenches (32) with said first plurality of trenches (25) to a second depth having the level of gate conduits to be formed in a latter step,
covering the trench walls of the second plurality of trenches (32) with insulation,
refilling said second plurality of trenches (32) and said excavated portions of said first plurality of trenches (25) with a conductive material (11, 12), removing said conductive material from said excavated portions of said first plurality of trenches (25) to expose the surfaces of said insulating material (17') therein and from alternating ones of said refilled second plurality of trenches (32) to a depth below said second depth to form a plurality of flat topped regions of said conductive (11) and said insulating materials which extend in a direction orthogonal to the direction of said first plurality of trenches (25),
forming insulating regions (10) at the top of said plurality of flat topped regions of conductive material such that the tops of the resulting insulation regions (10) are at the same level as the tops of said flat topped regions of insulating material thereby forming a plurality of gate conduits extending in a direction orthogonal to the direction of said first plurality of trenches (25).

2. A process according to claim 1 wherein in said first semiconductor substrate (21) being of a first conductivity type a layer (22) of second conductivity type is provided extending from the surface of said first substrate (21) partially into said first substrate (21) and wherein said underlying substrate (8) is also of first conductivity type.

3. A process according to claim 1 or 2 further including the steps of forming a pair of gate conductors (6) in each of said gate conduits in insulated spaced relationship with adjacent of said upstanding semiconductor regions,
depositing insulating material (15) in each of said gate conduits to electrically isolate the gate conductors (6) in each gate conduit from each other,
introducing a conductivity determining dopant into the top part of said upstanding semiconductor regions to form doped device regions,
planarizing said insulating material (15), and
forming a plurality of conductors (16) disposed in orthogonal relationship with said gate conductors (6) each of said conductors (16) contacting said doped device regions.

4. A process according to any one of claims 1 to 3 wherein the step of forming the first plurality of insulation filled trenches includes the steps of:
masking the said surface of said first semiconductor substrate (21) to expose portions of said surface,
etching said substrate to form said plurality of trenches (25) and
chemically vapor depositing said insulating material into said first plurality of insulation filled trenches.

5. A process according to any one of claims 1 to 4 wherein the step of forming the second plurality of trenches (32) and simultaneously excavating portions of said insulating material includes the steps of:
forming layers of a nitride, oxide and a nitride in that order on said surface and over said insulation filled trenches (25),
patterning said last mentioned nitride layer leaving spaced apart nitride masking regions,
depositing a layer of polycrystalline semiconductor conformally over said spaced apart nitride regions and reactively ion etching said polycrystalline semiconductor to form sidewall spacers on the sides of each of

said spaced apart nitride masking regions,
removing said spaced apart masking regions,
patterning said first mentioned nitride layer and said oxide layer to expose surface portions of said substrate (21) and said insulation filled trenches (25), and,
reactively ion etching said exposed surface portion of said substrate (21) and said insulation filled trenches (25) to form said second plurality of trenches and excavated portions of said insulating material simultaneously.

6. A process according to anyone of claims 1 to 5 wherein the steps of covering the trench walls with insulation and refilling said trenches (32) and said excavated portions with conductive material (11, 12) includes the steps of:
forming a composite oxide-nitride layer and a protective layer of polycrystalline semiconductor in said second plurality of trenches (32),
subjecting said second plurality of trenches (32) to reactive ion etching to remove said protective layer of polycrystalline layer from said second plurality of trenches (32) and said composite oxide-nitride layer from the bottoms of said second plurality of trenches (32),
depositing polycrystalline semiconductor material in said second plurality of trenches (32) and in said excavated portions and,
polishing said semiconductor material to planarize the surface of said memory array.

7. A process according to any one of claims 1 to 6 wherein the step of removing said conductive material (11) from every other trench of said second plurality of trenches (32) filled with conductive material (11) includes the steps of:
reactively ion etching said every other trench (32) to form a plurality of trenches in said conductive material (11).

8. A process according to claim 7 wherein the step of forming insulation at the bottom of each of said trenches in said conductive material (11) includes the step of oxidizing the topmost portion of said conductive material (11).

9. An ultra dense dynamic random access memory (DRAM) array containing a plurality of DRAM cells which array comprises:
an at least semiconductive substrate (8, 11, 12) having a plurality of rows of DRAM cells (2) disposed in insulated spaced relationship with said substrate (8, 11, 12), said substrate having insulation regions (10) covering the top surfaces of substrate portions (11) which latter extend between pairs of DRAM cells (2) in each row and between insulation regions (17'), rows of which latter extend in the same direction as said rows of DRAM cells (2), the tops of said insulation regions (17') being level with the tops of said insulation regions (10), a plurality of elongated gate conduits extending perpendicular to said rows of DRAM cells (2) and formed on said insulating regions (10) and on the surfaces of said insulating regions (17'), a pair of gate electrodes (6) disposed in each of said gate conduits and oriented therewith, each one of said pairs of gate electrodes being in insulated spaced relationship with the other one of said pair and with a portion (4) each of said DRAM cells (2) further having an extended region (5) disposed in insulated spaced relationship with said substrate and beneath said portion (4), and a plurality of conductive lines (16) disposed orthogonally with said gate electrodes (6), each of said conductive lines contacting another portion (3) of each DRAM cell (2) in the same row.

10. A dynamic random access memory array according to claim 9 wherein said DRAM cells are field effect transistors.

11. A dynamic random access memory array according to claim 9 or 10 wherein said portion (4) of said DRAM cell is the channel region of a field effect transistor, and wherein said region (5) and said another portion (3) of said DRAM cell are drain and source regions, respectively, of said field effect transistor.

Patentansprüche

1. Verfahren zur Herstellung einer ultradichten DRAM-Speichermatrix, die eine Mehrzahl von DRAM-Zellen enthält, wobei das Verfahren folgende Schritte beinhaltet:
Bilden einer ersten Mehrzahl von Gräben (25) in einem Halbleitersubstrat (21), das von einem darunter-

liegenden - wenigstens halbleitenden - Substrat (8) durch eine isolierende Schicht (20) mit Abstand angeordnet ist, wobei sich die Gräben (25) durch das Halbleitersubstrat (21) und die isolierende Schicht (20) hindurch in das darunterliegende Substrat (8) hinein erstrecken,
Wiederauffüllen der Mehrzahl von Gräben (25) mit einem isolierenden Material (17),
Bilden einer zweiten Mehrzahl von Gräben (32), welche die erste Mehrzahl von Gräben (25) senkrecht kreuzen, wobei sich die Gräben (32) durch das Halbleitersubstrat (21) und die isolierende Schicht (20) hindurch in das darunterliegende Substrat (8) hinein bis in eine vorgegebene Tiefe erstrecken, wobei die erste beziehungsweise die zweite Mehrzahl von Gräben (25, 32) eine Mehrzahl von hervorstehenden Halbleiterbereichen zur Bildung der aktiven Bauelementbereiche der DRAM-Zellen definieren und wobei bei der Bildung der zweiten Mehrzahl von Gräben (32) Bereiche des isolierenden Materials (17), das die erste Mehrzahl von Gräben (25) füllt, an den Kreuzungsstellen der zweiten Mehrzahl von Gräben (32) mit der ersten Mehrzahl von Gräben (25) bis zu einer zweiten Tiefe, die auf der Höhe von in einem späteren Schritt zu bildenden Gatekanälen liegt, ausgespart werden,
Bedecken der Grabenwände der zweiten Mehrzahl von Gräben (32) mit einer Isolierung,
Wiederauffüllen der zweiten Mehrzahl von Gräben (32) und der ausgesparten Bereiche der ersten Mehrzahl von Gräben (25) mit einem leitfähigen Material (11, 12), Entfernen des leitfähigen Materials von den ausgesparten Bereichen der ersten Mehrzahl von Gräben (25), um die Oberflächen des isolierenden Materials (17') darin freizulegen, und von alternierenden der wiederaufgefüllten zweiten Mehrzahl von Gräben (32) bis zu einer Tiefe unterhalb der zweiten Tiefe, um eine Mehrzahl von Bereichen mit flacher Oberseite aus dem leitfähigen (11) und dem isolierenden Material zu bilden, die sich in eine Richtung senkrecht zu der Richtung der ersten Mehrzahl von Gräben (25) erstrecken,
Bilden von isolierenden Bereichen (10) an der Oberseite der Mehrzahl von Bereichen mit flacher Oberseite aus leitfähigem Material derart, daß die Oberseiten der resultierenden Isolationsbereiche (10) auf der gleichen Höhe liegen wie die Oberseiten der Bereiche mit flacher Oberseite aus isolierendem Material, wodurch eine Mehrzahl von Gatekanälen gebildet wird, die sich in eine Richtung senkrecht zu der Richtung der ersten Mehrzahl von Gräben (25) erstrecken.

2. Verfahren nach Anspruch 1, wobei in dem ersten Halbleitersubstrat (21), das von einem ersten Leitfähigkeitstyp ist, eine Schicht (22) vom zweiten Leitfähigkeitstyp vorgesehen ist, die sich von der Oberfläche des ersten Substrates (21) teilweise in das erste Substrat (21) hinein erstreckt, und wobei das darunterliegende Substrat (8) ebenfalls vom ersten Leitfähigkeitstyp ist.

3. Verfahren nach Anspruch 1 oder 2, das des weiteren folgende Schritte einschließt:
Bilden eines Paares von Gateleitern (6) in jedem der Gatekanäle isoliert mit Abstand angrenzend an die hervorstehenden Halbleiterbereiche angeordnet,
Abscheiden von isolierendem Material (15) in jedem der Gatekanäle, um die Gateleiter (6) in jedem Gatekanal elektrisch voneinander zu isolieren,
Einbringen eines die Leitfähigkeit bestimmenden Dotierstoffes in den oberen Teil der hervorstehenden Halbleiterbereiche, um dotierte Bauelementbereiche zu erzeugen,
Ebnen des isolierenden Materials (15), und
Bilden einer Mehrzahl von Leitern (16), die senkrecht zu den Gateleitern (6) angeordnet sind, wobei jeder der Leiter (16) die dotierten Bauelementbereiche kontaktiert.

4. Verfahren nach einem der Ansprüche 1 bis 3, wobei der Schritt zum Bilden der ersten Mehrzahl von mit einer Isolierung gefüllten Gräben folgende Schritte einschließt:
Maskieren der Oberfläche des ersten Halbleitersubstrates (21), um Bereiche der Oberfläche freizulegen,
Ätzen des Substrates, um eine Mehrzahl von Gräben (25) zu erzeugen, und
chemische Gasphasenabscheidung des isolierenden Materials in die erste Mehrzahl von mit einer Isolierung gefüllten Gräben hinein.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei der Schritt zum Bilden der zweiten Mehrzahl von Gräben (32) und zum gleichzeitigen Aussparen von Bereichen des isolierenden Materials folgende Schritte einschließt:
Bilden von Schichten aus einem Nitrid, einem Oxid und einem Nitrid in dieser Reihenfolge auf der Oberfläche und über den mit einer Isolierung gefüllten Gräben (25),
Strukturieren der letzten erwähnten Nitridschicht, wobei voneinander mit Abstand angeordnet Maskierungsbereiche aus Nitrid zurückbleiben,
konformes Aufbringen einer Schicht aus einem polykristallinen Halbleiter über den voneinander mit Ab-

stand angeordneten Nitridbereichen und reaktives Ionenätzen des polykristallinen Halbleiters, um Seitenwandabstandshalter an den Seiten jedes der voneinander beabstandeten Maskierungsbereiche aus Nitrid zu bilden,
Entfernen der voneinander mit Abstand angeordneten Maskierungsbereiche,
Strukturieren der ersten erwähnten Nitridschicht und der Oxidschicht, um Oberflächenbereiche des Substrates (21) und der mit einer Isolierung gefüllten Gräben (25) freizulegen, und
reaktives Ionenätzen des freigelegten Oberflächenbereiches des Substrates (21) und der mit einer Isolierung gefüllten Gräben (25), um die zweite Mehrzahl von Gräben und gleichzeitig ausgesparte Bereiche des isolierenden Materials zu erzeugen.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei die Schritte zum Bedecken der Grabenwände mit einer Isolierung und zum Wiederauffüllen der Gräben (32) und der ausgesparten Bereiche mit leitfähigem Material (11, 12) folgende Schritte einschließen:
Bilden einer zusammengesetzten Oxid-Nitrid-Schicht und einer Schutzschicht aus einem polykristallinen Halbleiter in der zweiten Mehrzahl von Gräben (32),
Einwirken auf die zweite Mehrzahl von Gräben (32) mit einem reaktiven Ionenätzvorgang, um die Schutzschicht aus einer polykristallinen Schicht von der zweiten Mehrzahl von Gräben (32) und die zusammengesetzte Oxid-Nitrid-Schicht von den Böden der zweiten Mehrzahl von Gräben (32) zu entfernen,
Aufbringen von polykristallinem Halbleitermaterial in der zweiten Mehrzahl von Gräben (32) und in den ausgesparten Bereichen und
Polieren des Halbleitermaterials, um die Oberfläche der Speichermatrix zu ebnen.

7. Verfahren nach einem der Ansprüche 1 bis 6, wobei der Schritt zum Entfernen des leitfähigen Materials (11) von jedem zweiten Graben der zweiten Mehrzahl von Gräben (32), gefüllt mit leitfähigem Material (11), folgende Schritte einschließt:
reaktives Ionenätzen jedes zweiten Grabens (32), um eine Mehrzahl von Gräben in dem leitfähigen Material (11) zu erzeugen.

8. Verfahren nach Anspruch 7, wobei der Schritt zum Bilden einer Isolierung am Boden von jedem der Gräben in dem leitfähigen Material (11) den Schritt zum Oxidieren des obersten Bereiches des leitfähigen Materials (11) einschließt.

9. Ultradichte Matrix aus dynamischen Speichern mit wahlfreiem Zugriff (DRAM), die eine Mehrzahl von DRAM-Zellen enthält, wobei die Matrix folgendes beinhaltet:
ein wenigstens halbleitendes Substrat (8, 11, 12) mit einer Mehrzahl von Zeilen aus DRAM-Zellen (2), die bezüglich des Substrates (8, 11, 12) isoliert mit Abstand angeordnet sind, wobei das Substrat Isolationsbereiche (10) aufweist, welche die Oberseiten der Substratbereiche (11) bedecken, wobei sich die letzteren zwischen Paaren von DRAM-Zellen (2) in jeder Zeile und zwischen Isolationsbereichen (17') erstrecken, wobei sich Zeilen der letzteren in der gleichen Richtung wie die Zeilen der DRAM-Zellen (2) erstrecken, wobei die Oberseiten der Isolationsbereiche (17') auf gleicher Höhe wie die Oberseiten der Isolationsbereiche (10) liegen, wobei sich eine Mehrzahl von langgestreckten Gatekanälen senkrecht zu den Zeilen der DRAM-Zellen (2) erstreckt und auf den isolierenden Bereichen (10) sowie auf den Oberflächen der isolierenden Bereiche (17') ausgebildet ist, wobei ein Paar von Gate-Elektroden (6) in jedem der Gatekanäle angeordnet und dazu orientiert ist, wobei in jedem der Paare von Gate-Elektroden die eine isoliert mit Abstand zu der anderen des Paares liegt, wobei ein Bereich (4) jeder der DRAM-Zellen (2) des weiteren einen ausgedehnten Bereich (5) aufweist, der bezüglich des Substrates isoliert mit Abstand und unterhalb des Bereiches (4) angeordnet ist, wobei eine Mehrzahl von leitfähigen Bahnen (16) orthogonal zu den Gate-Elektroden (6) angeordnet ist und wobei jede der leitfähigen Bahnen einen anderen Bereich (3) jeder DRAM-Zelle (2) in der gleichen Zeile kontaktiert.

10. Matrix aus dynamischen Speichern mit wahlfreiem Zugriff nach Anspruch 9, wobei die DRAM-Zellen Feldeffekttransistoren sind.

11. Matrix aus dynamischen Speichern mit wahlfreiem Zugriff nach Anspruch 9 oder 10, wobei der Bereich (4) der DRAM-Zelle der Kanalbereich eines Feldeffekttransistors ist und wobei der Bereich (5) und der weitere Bereich (3) der DRAM-Zelle Drain- beziehungsweise Sourcebereiche des Feldeffekttransistors sind.

Revendications

1. Procédé de fabrication d'une matrice de mémoire ultra-dense du type DRAM contenant une pluralité de cellules DRAM, lequel procédé comprend les étapes de:

former une première pluralité de tranchées (25) dans un substrat semiconducteur (21) qui est écarté d'un substrat sous-jacent -au moins semiconducteur- (8) par une couche isolante (20), lesdites tranchées (25) traversant ledit substrat semiconducteur (21) et ladite couche isolante (20) pour pénétrer dans ledit substrat sous-jacent (8),

remplir à nouveau ladite pluralité de tranchées (25) d'un matériau isolant (17),

former une deuxième pluralité de tranchées (32) faisant orthogonalement intersection avec ladite première pluralité de tranchées (25), lesdites tranchées (32) traversant ledit substrat semiconducteur (21) et ladite couche isolante (20) pour pénétrer dans ledit substrat sous-jacent (8) sur une profondeur prédéterminée, lesdites première et deuxième pluralité de tranchées (25, 32) définissant respectivement une pluralité de régions semiconductrices droites pour former les régions de dispositif actives desdites cellules DRAM et, durant la formation de ladite deuxième pluralité de tranchées (32), des portions dudit matériau isolant (17) remplissant ladite première pluralité de tranchées (25) étant creusées aux intersections de ladite deuxième pluralité de tranchées (32) avec ladite première pluralité de tranchées (25) sur une deuxième épaisseur ayant le niveau de conduits de porte à former dans une étape ultérieure,

couvrir les parois de tranchée de la deuxième pluralité de tranchées (32) d'un isolant,

remplir à nouveau ladite deuxième pluralité de tranchées (32) et lesdites portions creusées de ladite première pluralité de tranchées (25) d'un matériau conducteur (11, 12),

enlever ledit matériau conducteur desdites portions creusées de ladite première pluralité de tranchées (25) pour y exposer les surfaces dudit matériau isolant (17'), et desdites tranchées alternées de ladite deuxième pluralité de tranchées remplie à nouveau (32) sur une profondeur en dessous de ladite deuxième profondeur pour former une pluralité de régions à sommet plat dudit matériau conducteur (11) et desdits matériaux isolants qui se prolongent dans une direction orhtogonale à la direction de ladite première pluralité de tranchées (25),

former des régions isolantes (10) au sommet de ladite pluralité de régions à sommet plat de matériau conducteur de sorte que les sommets des régions isolantes obtenues finalement (10) soient au même niveau que les sommets desdites régions à sommet plat de matériau isolant, formant de ce fait une pluralité de conduits de porte se prolongeant dans une direction orthogonale à la direction de ladite première pluralité de tranchées (25).

2. Procédé selon la revendication 1, dans lequel, dans ledit premier substrat conducteur (21) qui est d'un premier type de conductivité (22), il est fourni une couche (22) d'un deuxième type de conductivité qui s'étend depuis la surface dudit premier substrat (21) partiellement dans ledit premier substrat, et dans lequel ledit substrat sous-jacent (8) est également du premier type de conductivité.

3. Procédé selon les revendications 1 ou 2, comprenant en outre les étapes de:

former une paire de conducteurs de porte (6) dans chacun desdits conduits de porte en relation isolée espacée avec les régions adjacentes desdites régions semiconductrices droites,

déposer le matériau isolant (15) dans chacun desdits conduits pour isoler électriquement entre eux les conducteurs de porte (6) dans chaque conduit de porte,

introduire un dopant de détermination de conductivité dans la partie supérieure desdites régions semiconductrices droites pour former des régions de dispositif dopées,

aplanir ledit matériau isolant (15), et

former une pluralité de conducteurs (16) disposés en relation orthogonale avec lesdits conducteurs de porte (6), chacun desdits conducteurs (16) faisant contact avec lesdites régions de dispositif dopées.

4. Procédé selon l'une quelconque des revendications 1 à 3, dans lequel l'étape de former la première pluralité de tranchées remplie d'isolant, comprend les étapes de:

masquer ladite surface dudit premier substrat semiconducteur (21) pour exposer des portions de ladite surface,

décaper ledit substrat pour former ladite pluralité de tranchées (25), et

déposer chimiquement en phase vapeur ledit matériau isolant dans ladite première pluralité de tranchées remplie d'isolant.

5. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel l'étape de former ladite deuxième

pluralité de tranchées (32) et de creuser simultanément des portions dudit matériau isolant, comprend les étapes de:

former des couche de nitrure, d'oxyde et de nitrure, dans cet ordre, sur ladite surface et sur lesdites tranchées remplies d'isolant (25),

configurer ladite couche de nitrure dernièrement mentionnée en laissant écartées des régions de masquage de nitrure,

déposer une couche de semiconducteur polycristallin en se conformant auxdites régions de nitrure écartées et décaper par ions réactifs ledit semiconducteur polycristallin pour former des entretoises de paroi latérale sur les côtés de chacune desdites régions de masquage de nitrure écartées,

enlever lesdites régions de masquage écartées,.

configurer ladite première couche de nitrure mentionnée et ladite couche d'oxyde pour exposer des portions de surface dudit substrat (21) et lesdites tranchées remplies d'isolant (25), et

décaper par ions réactifs ladite portion de surface exposée dudit substrat (21) et lesdites tranchées remplies d'isolant (25) pour former simultanément lesdites deuxième pluralité de tranchées et portions creusées dudit matériau isolant.

6. Procédé selon l'une quelconque des revendications 1 à 5, dans lequel les étapes de couvrir les parois de tranchée d'un isolant et de remplir à nouveau lesdites tranchées (32) et lesdites portions creusées d'un matériau conducteur (11, 12), comprend les étapes de:

former une couche composite d'oxyde-nitrure et une couche de protection de semiconducteur polycristallin dans ladite deuxième pluralité de tranchées (32),

soumettre ladite deuxième pluralité de tranchées (32) à un décapage par ions réactifs pour enlever ladite couche de protection de couche polycristalline de ladite deuxième pluralité de tranchées (32) et ladite couche composite d'oxyde-nitrure du bas de ladite deuxième pluralité de tranchées (32),

déposer le matériau semiconducteur polycristallin dans ladite deuxième pluralité de tranchées (32) et dans lesdites portions creusées, et

polir ledit matériau semiconducteur pour aplanir la surface de ladite matrice de mémoire.

7. Procédé selon l'une quelconque des revendications 1 à 6, dans lequel l'étape d'enlever ledit matériau conducteur (11) d'une tranchée sur deux de ladite deuxième pluralité de tranchées (32) remplies de matériau conducteur (11), comprend les étapes de:

décaper par ions réactifs ladite une tranchée sur deux (32) pour former une pluralité de tranchées dans ledit matériau conducteur (11).

8. Procédé selon la revendication 7, dans lequel l'étape de former l'isolation au bas de chacune desdites tranchées dans ledit matériau conducteur (11), comprend l'étape d'oxyder la portion supérieure dudit matériau conducteur (11).

9. Matrice de mémoire à accès direct dynamique ultra-dense (DRAM) contenant une pluralité de cellules DRAM, ladite matrice comprenant:

au moins un substrat semiconducteur (8, 11, 12) ayant une pluralité de rangées de cellules DRAM (2) disposées en relation isolée espacée avec ledit substrat (8, 11, 12), ledit substrat ayant des régions d'isolation (10) couvrant les surfaces supérieures des portions de substrat (11) lesquelles s'étendent entre des paires de cellules DRAM (2) dans chaque rangée et entre des régions d'isolation (17') dont des rangées s'étendent dans la même direction que lesdites rangées de cellules DRAM (2), le haut desdites régions d'isolation (17') étant au niveau du haut desdites régions d'isolation (10), une pluralité de conduits de porte allongés s'étendant perpendiculairement auxdites rangées de cellules DRAM (2) et formés sur lesdites régions isolantes (10) et sur les surfaces desdites régions d'isolation (17'), une paire d'électrodes de porte (6) disposées dans chacun desdits conduits de porte et orientées avec ces derniers, chacune desdites paires d'électrodes de porte étant en relation isolée espacée avec l'autre de ladite paire et avec une portion (4), chacune desdites cellules DRAM (2) ayant en outre une région étendue (5) disposée en relation isolée espacée avec ledit substrat et dessous ladite portion (4), et une pluralité de ligne conductrices (16) disposées orthogonalement avec lesdites électrodes de porte (6), chacune desdites lignes conductrices faisant contact avec une autre portion (3) de chaque cellule DRAM (2) dans la même rangée.

10. Matrice de mémoire à accès direct dynamique selon la revendication 9, dans laquelle lesdites cellules DRAM sont des transistors à effet de champ.

11. Matrice de mémoire à accès direct selon les revendications 9 ou 10, dans laquelle ladite portion (4) de

ladite cellule DRAM est la région de canal d'un transistor à effet de champ, et dans laquelle ladite région (5) et ladite une autre portion (3) de ladite cellule DRAM sont respectivement les régions de drain et de source dudit transistor à effet de champ.

FIG. 1

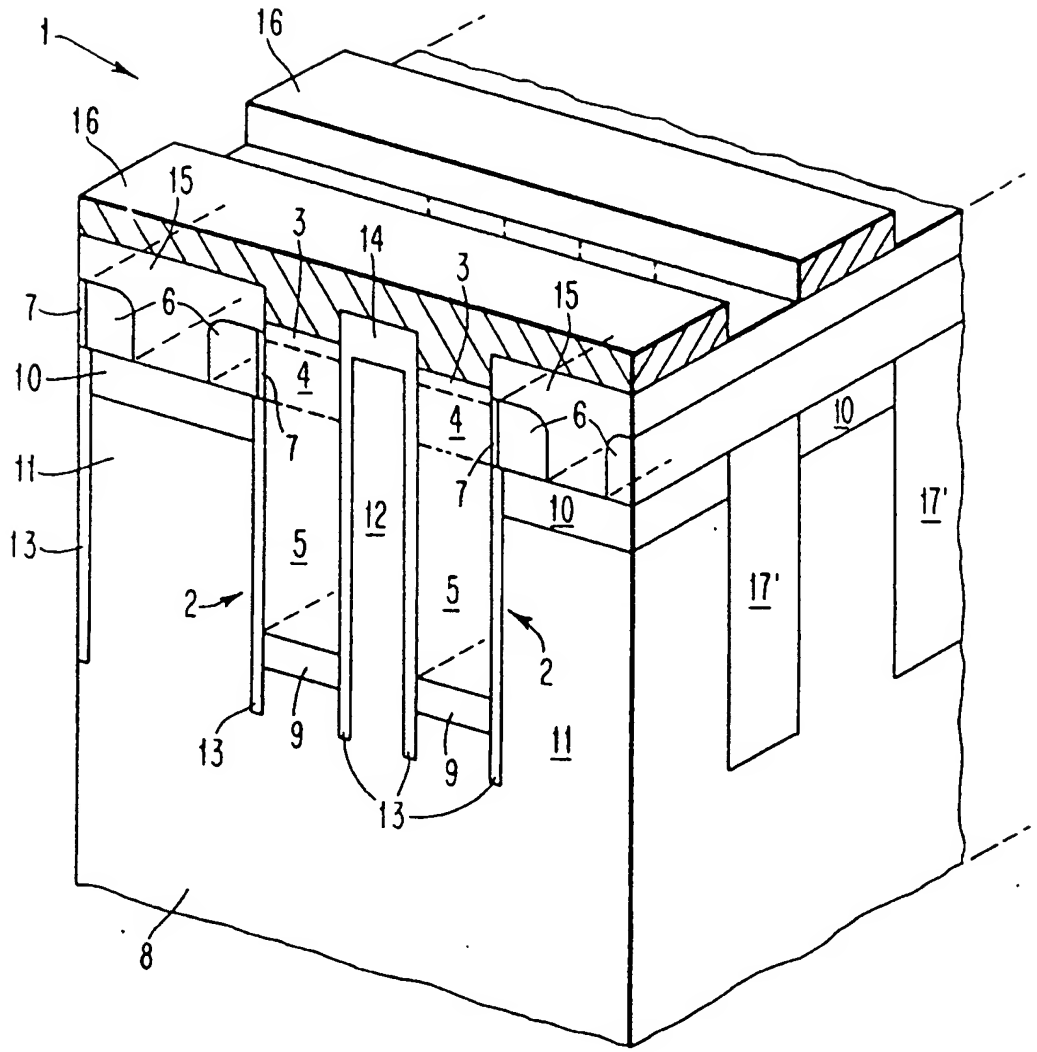

FIG. 2

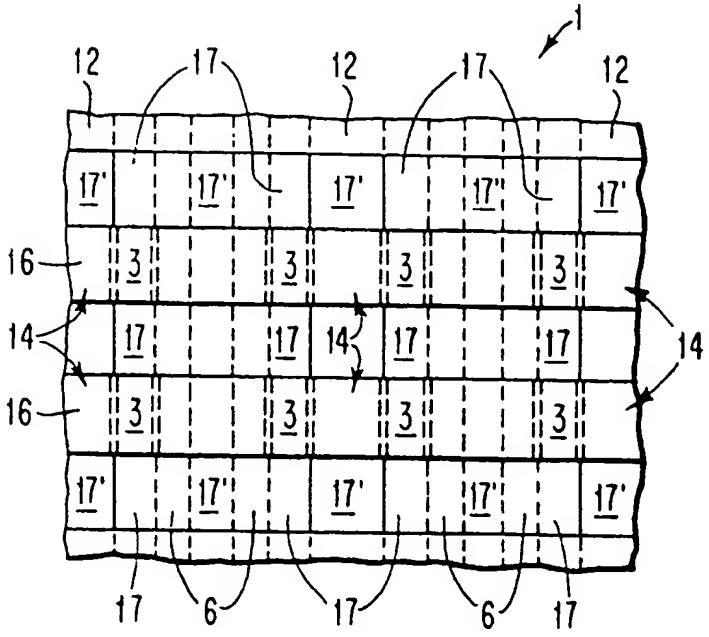
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FIG. 3

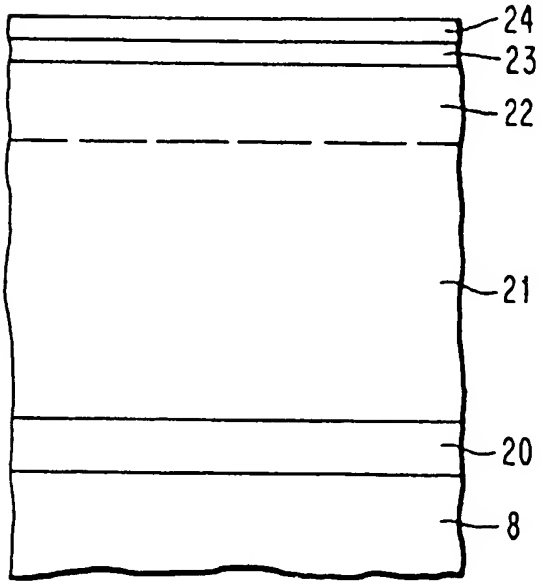
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FIG. 4

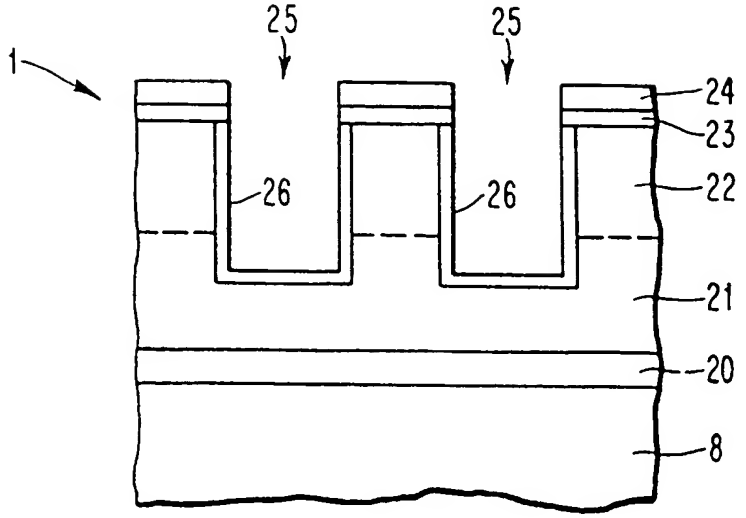

FIG. 5

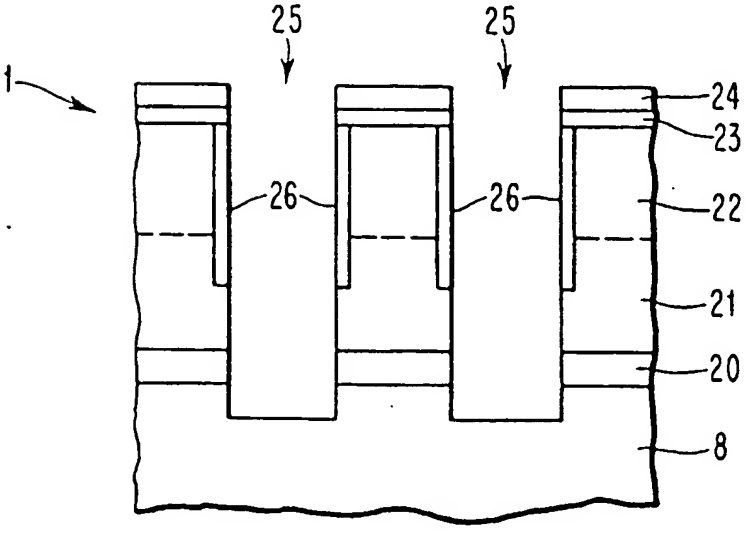

FIG. 6

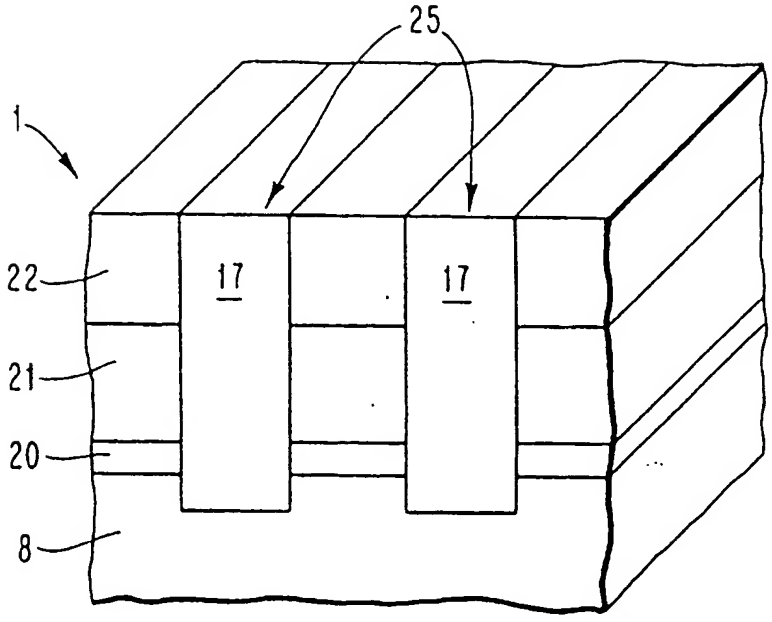

FIG. 7

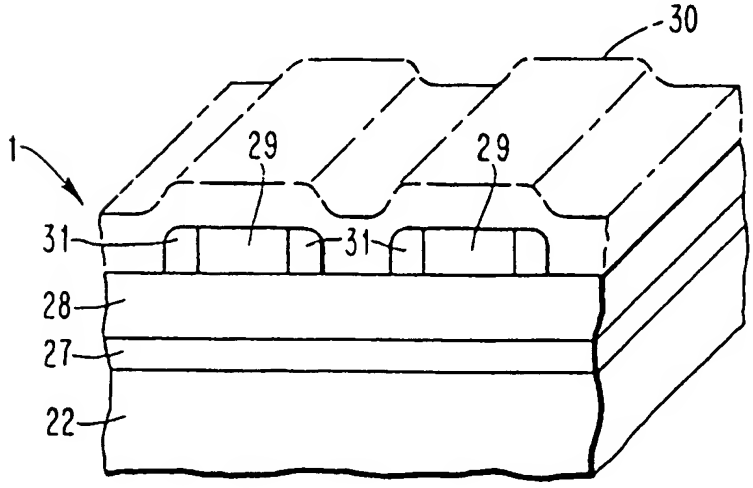

FIG. 8

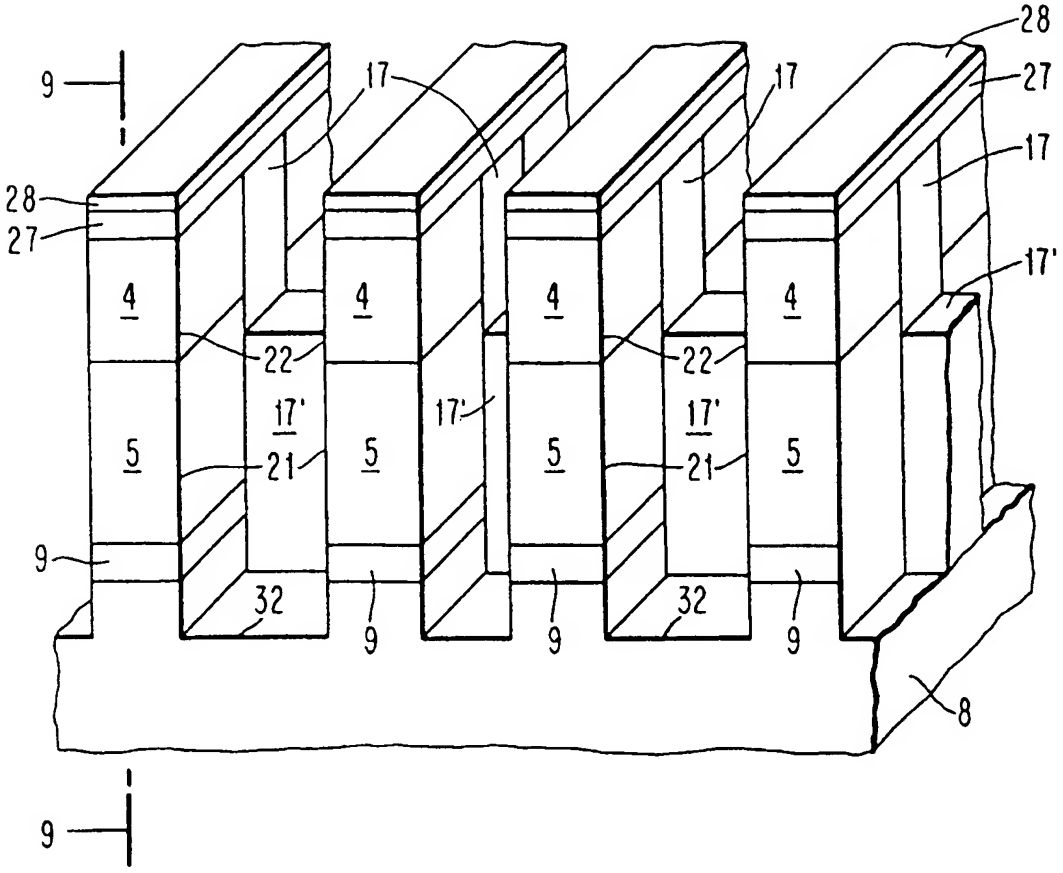
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FIG. 9

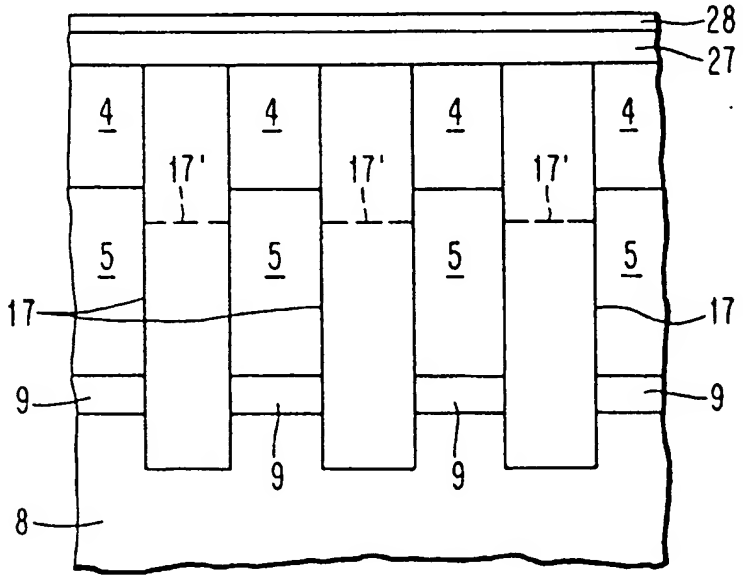
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FIG. 10

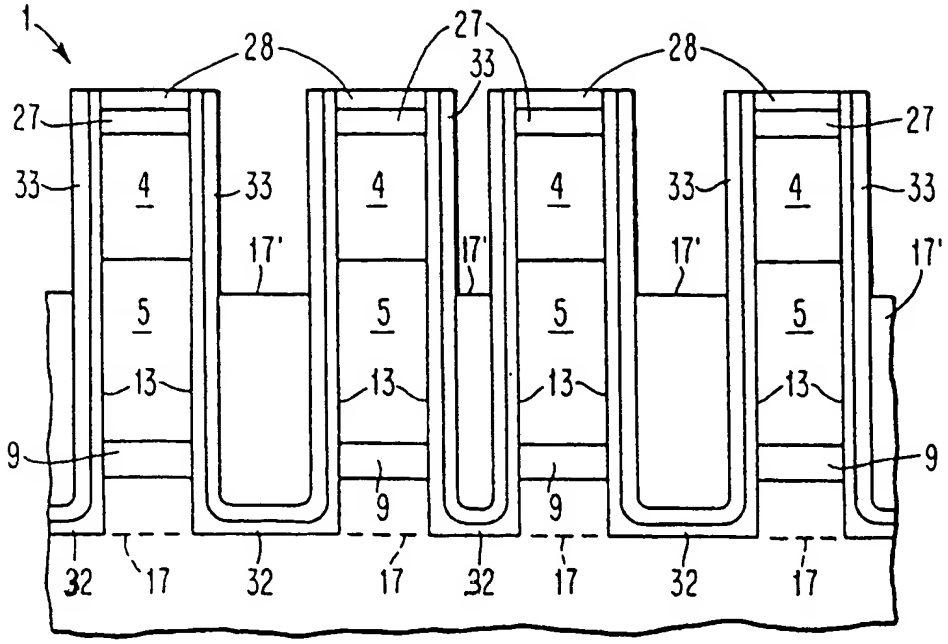
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FIG. 11

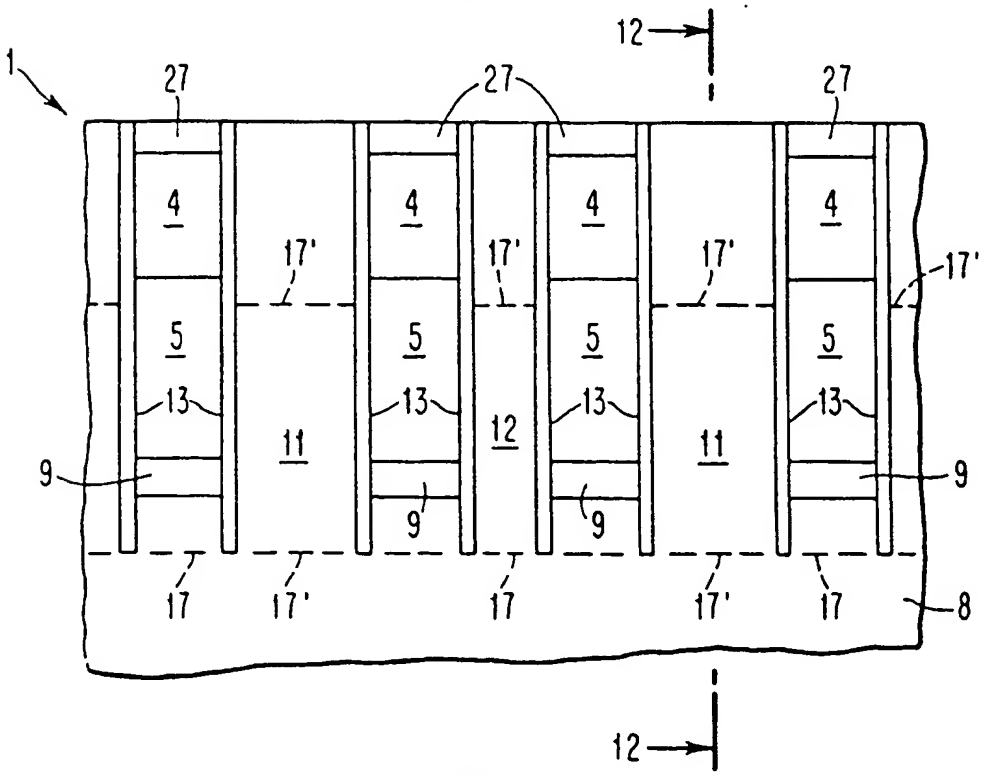
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FIG. 12

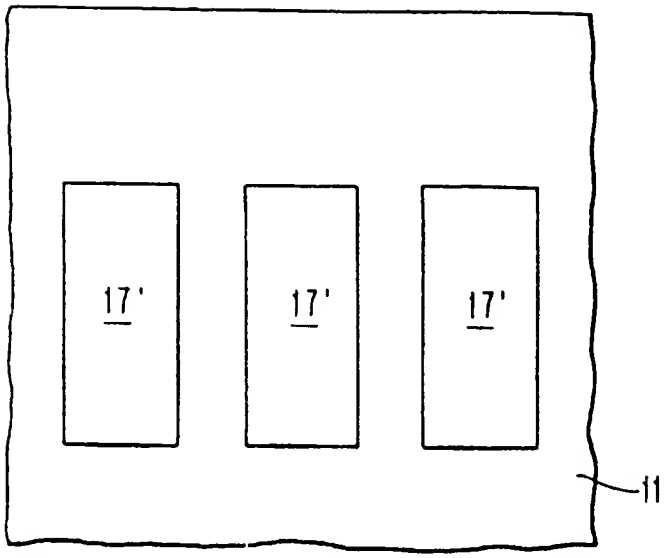
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FIG. 13

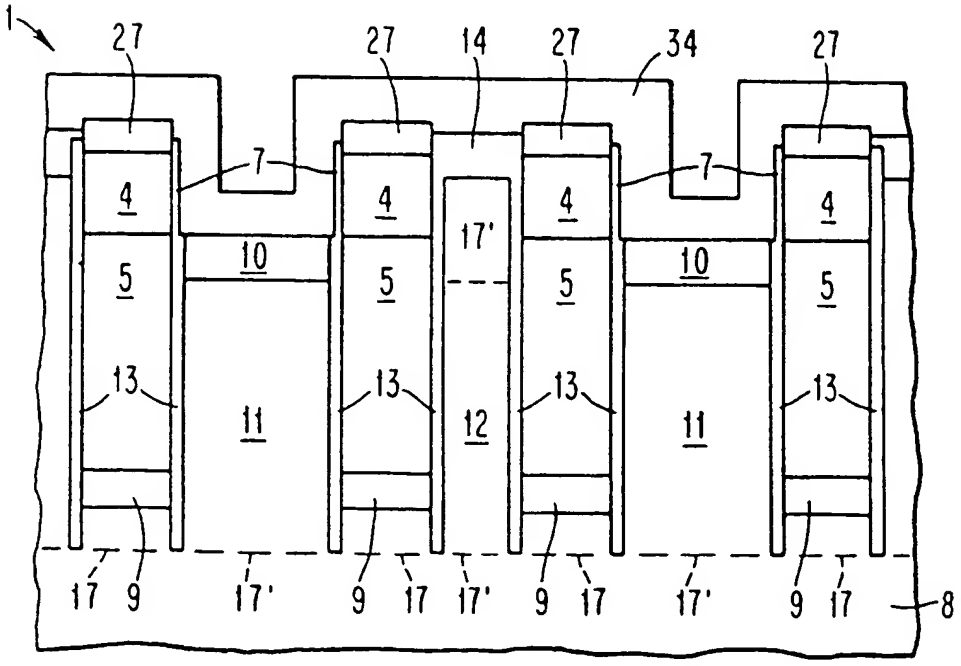
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FIG. 14

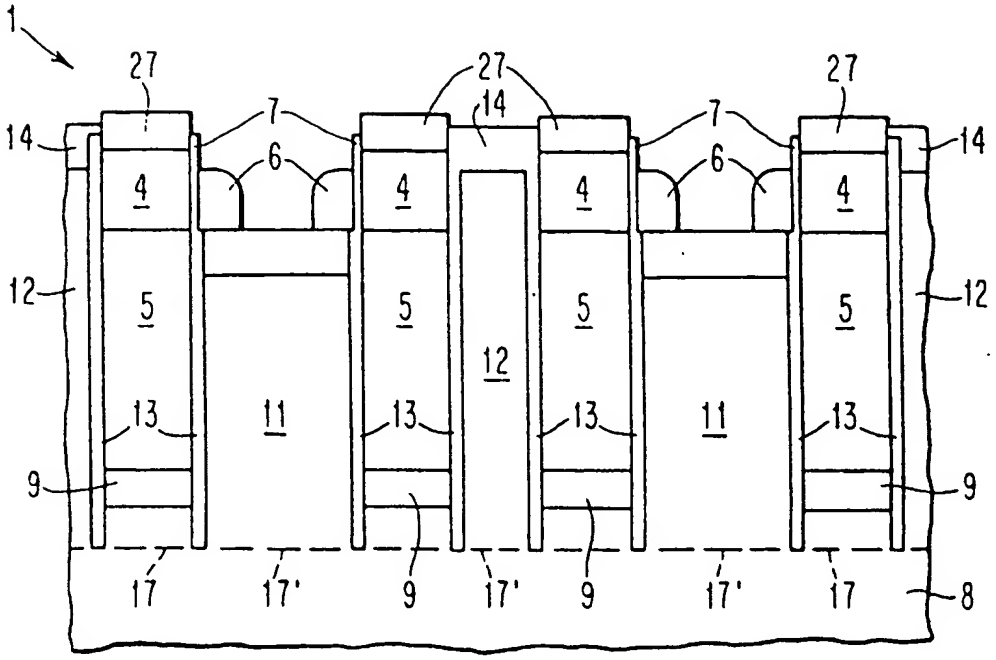
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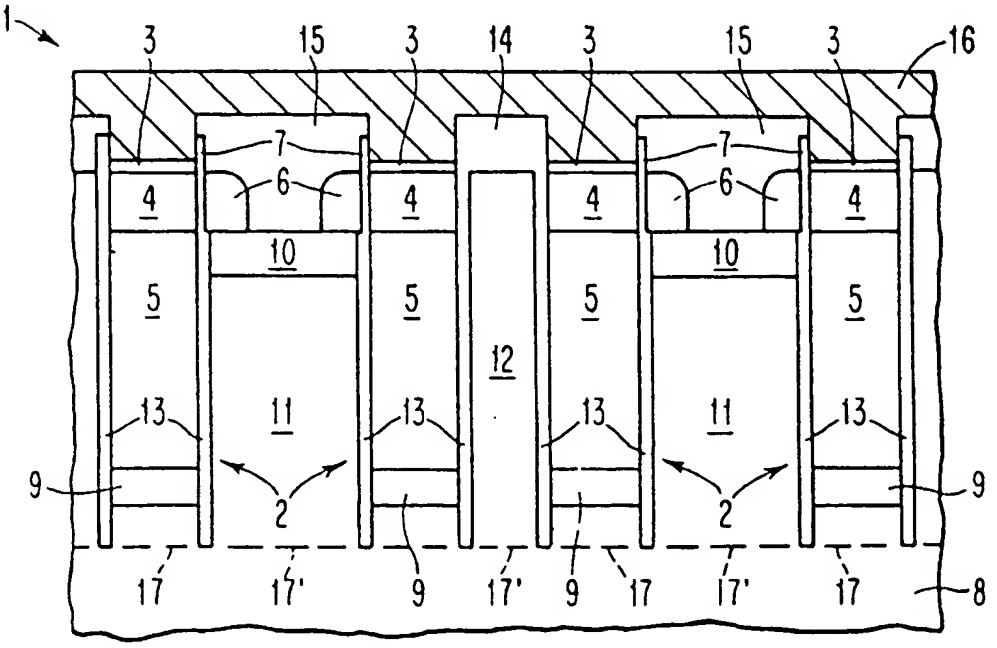
FIG. 15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